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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/109,261
Filing Date	June 30, 1998
First Named Inventor	Gang Bai
Art Unit	2815
Examiner Name	Warren, Matthew E.
Attorney Docket Number	42390P5769

Total Number of Pages in This Submission: 18

ENCLOSURES *(check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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- [ ] CD, Number of CD(s)
- [ ] After Allowance Communication to Group
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	William Thomas Babbitt, Reg. No. 39,591 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	William T Babbitt
Date	11/2/05

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Nedy Calderon		
Signature	Nedy Calderon	Date	11/2/05

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FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($) 0.00

Complete if Known	
Application Number	09/109,261
Filing Date	June 30, 1998
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METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☒ None ☐ Other (please identify): ______

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below

☐ Charge fee(s) indicated below, except for the filing fee

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FEE CALCULATION

1. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	10	- 20** =	0	x	50.00	=	$0.00
Independent Claims	2	- 3** =	0	x	200.00	=	$0.00
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple Dependent claim, if not paid
1204	300	2204	150	**Reissue independent claims over original patent
1205	300	2205	150	**Reissue claims in excess of 20 and over original patent

***or number previously paid, if greater, For Reissues, see below*

SUBTOTAL (1) ($) 0.00

2. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify)					

SUBTOTAL (2) ($)

SUBMITTED BY				Complete (if applicable)	
Name *(Print/Type)*	William Thomas Babbitt	Registration No. *(Attorney/Agent)*	39,591	Telephone	(310) 207-3800
Signature	William T Babbitt			Date	11/2/05

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Our Ref. No.: 042390.P5769

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	
Gang Bai	Examiner: **Warren, Matthew E.**
Application No.: **09/109,261**	Art Unit: **2815**
Filed: **June 30, 1998**	
For: **A MULTI-LAYER GATE DIELECTRIC**	

AMENDED APPEAL BRIEF

Mail Stop Appeal Brief - Patent
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notification of Non-Compliant Appeal Brief mailed October 19, 2005, Applicants submit the following Amended Appeal Brief pursuant to 37 C.F.R. § 41.37 for consideration by the Board of Patent Appeals and Interferences. Please charge any additional amount due or credit any overpayment to the Deposit Account 02-2666.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Gang Bai, the party named in the caption, transferred his rights to the subject Application through an assignment recorded on August 25, 1998 (Reel/Frame 9424/0287) in the patent application to Intel Corporation, of Santa Clara, California. Thus, as the owner at the time the brief is being filed, Intel Corporation is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences that will affect or be affected by the outcome of this appeal.

III. STATUS OF CLAIMS

Claims 8-10, 13-17 and 20-21 are pending and rejected in the Application. Applicant hereby appeals the rejection of all pending claims.

IV. STATUS OF AMENDMENTS

The claims are amended in accordance with an Amendment and Response to Office Action filed June 7, 2004. The claim amendments presented at that time were entered. Accordingly, the claims stand as amended June 7, 2004.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

In one aspect, a transistor device and an apparatus including a semiconductor substrate having a transistor device formed thereon, wherein the transistor device includes a gate dielectric having increased capacitance over a traditional silicon dioxide gate dielectric and in another aspect may be consistent with scaling techniques associated with transistor or device sizial. Figure 1 illustrates an embodiment of a transistor device on a substrate including a multi-layer gate dielectric. Figure 1 shows transistor 100 consisting of gate electrode 110 overlying gate dielectric 140. See Application, page 7, lines18-19. Figure 1 shows transistor 100 consisting of gate electrode 110 overlying gate dielectric 140. See Application, page 7, lines 19-20. Gate electrode 110 and gate dielectric 140 overlie semiconductor substrate 105. See Application, page 7, lines 21-22. Formed in substrate 105 adjacent transistor gate electrode 110 are diffusion or junction regions 160. See Application, page 7, lines 23-24. The transistor device in Figure 1 is isolated from other devices by shallow trench isolation structures 150. See Application, page 7, line 24 through page 8, line 2.

Gate dielectric 140 in the embodiment illustrated in Figure 1, is made up of a multi-layer gate dielectric stack. See Application, page 8, lines 3-4. In one embodiment, gate dielectric 140 includes bottom dielectric layer 130 and top dielectric layer 120. Bottom dielectric layer 130 is a material with a modest dielectric constant, k_1. See Application, page 8, line 10-12. Examples of suitable material for bottom dielectric layer 130 include, but are not limited to, hafnium oxide (HfO_2), zirconium oxide (ZrO_2), barium oxide (BaO), lanthanum oxide (La_2O_3), and yttrium oxide (Y_2O_3). See Application, page 8, lines 23-26.

Top dielectric layer 120 in one embodiment, is selected to have a relatively high dielectric constant, k_2, and is a material that is generally stable in contact with gate electrode 110. See Application, page 9, lines 1-2. Examples of suitable top dielectric layers are barium, strontium, titanate (BST) and lead, zirconium titanate (PZT). See Application, page 9, lines 4-5.

One guideline to select an appropriate dielectric layer thickness, t_1 for bottom dielectric layer 130, and, t_2, for top dielctric 120 is that, for a given technology (e.g., given gate length of gate electrode 110 and equivalent oxide thickness of a silicon dioxide gate dielectric, t_{ox}, a total thickness, t, of gate dielectric 140 should be less than one-third of the gate length of gate electrode 110. See Application, page 9, lines 11-17. The effective dielectric constant, k, may then be determined by the following relationship:

$$k=k_{ox}(t/t_{ox}) \tag{1}$$

wherein k_{ox} is the dielectric constant of silicon dioxide which is typically represented as 4.0. See Application, page 9, lines 17-22. Combining the above relationship with a relationship for calculating the effective dielectric constant of gate dielectric 140 of

$$k=t/(t_1/k_1 + t_2/k_2), \tag{2}$$

the total thickness of dielectric layer 140 may be calculated:

$$t=t_1 + t_2 \tag{3}$$

See Application, page 9, line 23 through page 10 line 3. Combining equations (1), (2), (3) yields:

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox} \tag{4}$$

wherein t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length, k_{ox} is a dielectric constant of silicone dioxide. See Application, page 10, lines 4-5.

By manipulating the gate dielectric materials, the capacitance of the device may be appropriately increased for a given technology. See Application, page 10, line 23 through page 11, line 2. Scaling for a set of feature size technologies defined, for example, by gate lengths on the order of 25 to 70 nanometers is also contemplated. See Application, page 11, lines 17-20. In certain instances, a third dielectric layer may be utilized, such as barrier layer to prevent interaction

between top dielectric layer 120 materials and the gate electrode material. See Application, page 11, lines 3-9.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The ground of rejection in this appeal is:

Whether claims 8-10, 13-17m 20 and 21 are obvious under 35 U.S.C. §103(a) over U.S. Patent No. 4,015,281 issued to Nagata et al. (Nagata) in view of U.S. Patent No. 5,990,516 issued to Momose et al. (Momose) and U.S. Patent No. 5,621,681 issued to Moon (Moon).

VII. ARGUMENT

A. Overview of the Cited References

1. Nagata

Nagata describes an insulated-gate field effect transistor (MIS-FET), particularly an N-channel MIS-FET. Nagata describes in, in one embodiment, a semiconductor device comprising P-type semiconductor substrate, at least two N-channel insolated-gate field effect transistors (MIS-FETs) disposed on a surface of the semiconductor substrate in electrically isolated relation from each other, an isolating film means disposed on the surface portion of the semiconductor substrate between the N-channel MIS-FET and formed by plurality of films including a first film of insulator stable against various kinds of stress, a second film of insulator capable of inducing holes in the surface portion of the semiconductor substrate, and a third film of insulator having a low dielectric constant and a large effective oxide thickness to produce an induced hole layer of controlled impurity concentration in the surface portion of the semiconductor substrate for providing an isolation having a sufficiently high threshold voltage, V_{th}. See column 4, lines 10-32. Nagata defines its "effective oxide thickness" as follows:

$$T_{eff} = \left(\frac{T_{SiO_2}}{E_{SiO_2}} + \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet + \frac{T_{xi}}{E_{xi}} + \bullet\bullet\bullet \frac{T_{xn}}{E_{xn}} \right) E_{SiO_2}$$

Wherein Ts_io_2 and Es_io_2 are the thickness and dielectric constant respectively of a silicon dioxide film and T_{xi} and E_{xi} are the thickness and dielectric constant, respectively, of films other than the silicon dioxide film. See column 4, lines 32-49.

Nagata describes five different embodiments, each of which, according to Applicant's understanding, includes a gate dielectric material of silicon dioxide. See column 9, line 34 - column 15, line 35.

2. Momose

Momose discloses a ultra-high current drive metal oxide semiconductor (MOS) transistor. Momose notes that the current drive capability of a MOS field effects transistor (MOSFET) can be increased effectively by increasing the moving speed of electrons and holes, that is, by shortening the gate length and increasing the channel field strength. In one embodiment, Momose describes a MOSFET having a gate length of 0.15 microns and a gate oxide film thickness of less than 2.5 nanometers. See column 16, 9, lines 22-27. In addition to using a silicon oxide film as the gate insolating film, Momose describes the same effect can be obtained using various films, "for instance as follows: silicon nitrite film (Si_3N_4), silicon nitric oxide film (SiO_xN_y), a stacked films of silicon nitride film and silicon oxide film (SiO_2/Si_3N_4, Si_3N4/SiO_2, $SiO_2/Si_3N_4/SiO_2$, $Si_3N_4/SiO_2/N_4$), a lamenated layer of tantanum oxide (TaO_x), a titanium oxide strontrium ($TiSr_xO_y$) and its silicon oxide film or silicon nitride film, etc." Column 16, line 64 through column 17, line 11. When substituted insulating films are used, Momose teaches selecting film thicknesses to have a gate capacitance equivalent to a silicon film with a film thickness less than 2.5 nanometers. See column 17, lines 11-19. Momose does not define a total thickness of a multi-layer insulating film less than one-third of a length of the transistor gate.

With respect to its disclosure Momose states:

> Accordingly, the aforementioned transconductance and the current drive capability cannot be realized by the conventional methods so far reported, and can be realized in accordance with only the structure defined by the present invention

Column 15, lines 32-35. Thus, Momose concludes only its structure, and none of the teachings prior to its disclosure are suitable for producing a gate length of 40 nanometers or less.

3. Moon

Moon discloses a metal ferroelectric insulator semiconductor field effect transistor (MFISFET) having an insulating film that is matched in terms of lattice constant and thermal expansion coefficient with silicon. See column 2, lines 51-54. In Figure 2, a MFISFET memory device is shown including P-type silicon substrate 1, field oxide film 2 formed in a device isolation area, yttrium oxide (Y_2O_3) gate film 11A formed on a surface of substrate 1, ferroelectric gate film12A formed over the gate film 11A, a titanium nitride (T_1N) gate electrode 13A formed over

gate film 12A, and N-type source drain regions 3 formed in substrate 1 on opposite sides of gate electrode 13A.

B. Rejection of claims 8-10, 13-17 and 20-21 as obvious over Nagata in view of Momose and Moon

Regarding the rejection of claim 8, among other elements, claim 8 defines a transistor device having a gate electrode overlying a gate dielectric formed on a semiconductor substrate comprising a first and second dielectric material being scalable for a set of feature size technologies, the set of feature size technologies defined by a gate length in the range of 25-70 nanometers where the first material thickness and the second material thickness are determined by the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$ (see Equation 4, page 3 herein). According to the relationship, the sum of the thickness/dielectric constant of the first and second dialectric material must equal a thickness/dielectric constant for a gate dielectric of silicon dioxide.

The Patent Office notes the relationship in Nagata shown at col. 4, lines 39-44:

$$T_{eff} = \left(\frac{T_{SiO_2}}{E_{SiO_2}} + \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet + \frac{T_{xi}}{E_{xi}} + \bullet\bullet\bullet \frac{T_{xn}}{E_{xn}} \right) E_{SiO_2}$$

To arrive at the relationship set forth in claim 8 (Equation (4)), the Patent Office rewrites Nagata to solve for T_{eff}/E_{SiO_2}.

Applicant has performed the operation noted by the Patent Office. That operation is set forth below.

$$\frac{T_{eff}}{E_{SiO_2}} = \frac{T_{SiO_2}}{E_{SiO_2}} + \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet + \frac{T_{xi}}{E_{xi}} + \bullet\bullet\bullet \frac{T_{xn}}{E_{xn}}$$

$$\frac{T_{eff}}{E_{SiO_2}} - \frac{T_{SiO_2}}{E_{SiO_2}} = \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet + \frac{T_{xi}}{E_{xi}} + \bullet\bullet\bullet \frac{T_{xn}}{E_{xn}}$$

$$\frac{T_{eff} - T_{SiO_2}}{E_{SiO_2}} = \frac{T_{x1}}{E_{x1}} + \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet + \frac{T_{xi}}{E_{xi}} + \bullet\bullet\bullet \frac{T_{xn}}{E_{xn}} \qquad (5)$$

In comparing equation (5) to equation (4), the equations are not identical. They can be similar if $T_{eff}=0$ and T_{SiO_2} is a negative number, which does not appear realistic in either case. Alternatively, solving for T_{SiO_2}/E_{SiO_2}, the Momose relationship may be represented as follows:

$$\frac{T_{SiO_2}}{E_{SiO_2}} = \frac{T_{eff}}{E_{SiO_2}} - \frac{T_{x1}}{E_{x1}} - \frac{T_{x2}}{E_{x2}} \bullet\bullet\bullet - \frac{T_{xi}}{E_{xi}} \bullet\bullet\bullet - \frac{T_{xn}}{E_{xn}} \qquad (6)$$

According to this relationship, equation (6) and equation (4) are not the same. It follows that neither equation (5) or equation (6) are equivalent ot equation (4) in claim 8 since Nagata teaches the use of SiO_2 as a gate dielectric material.

Nagata teaches, "an enhancement and a depletion type metal-insulator-semiconductor field effect transistor being formed on a substrate of silicon and electrically isolated from each other by a plurality of layers including, for example, a first layer of SiO_2, a second layer of Al_2O_3 capable of inducing holes in the surface portion of the substrate, and third layer of SiO_2, and relation between the thickness of these layers is suitably selected for attaining satisfactory isolation between these transistors." See Nagata, abstract. Nagata does not teach or suggest a transistor device comprising a first dielectric material selected from one of HfO_2, BaO, La_2, O_3, Y_2O_3, and ZrO_2. Thus, Nagata fails to teach or suggest each of the elements of claim 8.

The Patent Office relies on Momose to cure certain defects of Nagata. Momose describes an insulating film for a MOSFET as including layers of silicon dioxide, or silicon dioxide, silicon nitride, silicon nitric oxide, stacks of silicon nitride and silicon oxide, or laminated layers of tantalum oxide, titanium oxide strontium and it silicon oxide or silicon nitride films. See Momose, column 16, line 66 through column 17, line 11. Momose fails to teach a relationship for material thickness for its dielectric materials similar to equation (4). Momose also fails to teach a transistor device comprising a first dielectric material selected from one of HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2 and thus fails to cure the defects of Nagata in this regard.

The Patent Office relies on Momose to teach a gate length of 40 nanometers and an insulating film less than one-third of the gate length. The Patent Office believes this teaching may be combined with that of Nagata. However, Momose specifically teaches specific structures utilizing specific materials that, at least in terms of the insulating film Momose does not include those materials specified for a first dielectric material in claim in 8 and does not describe how specific materials are scalable for a set of feature size technologies. Incorporating Momose into Nagata, does not follow that dielectric materials will have thicknesses determined by the relationship of equation (4).

Moon is cited for disclosing specific dielectric materials. Moon does not cure the defects of Nagata and Momose including a gate dielectric relationship relative to a particular thickness for a gate dielectric silicon dioxide or dielectric materials being scalable for a set of feature size technologies.

For the above stated reasons, claim 8 is not obvious over Nagata in view of Momose and Moon. Claims 9-10 and 13-14 depend from claim 8 and therefore contain all limitations of that

claim. For at least the reasons stated above, claim 9-10 and 13-14 are not obvious over the cited reference. In addition, claim 10 specifies a relationship between a gate length and dielectric thickness, i.e., the combination of a first thickness and a second thickness of dielectric materials is less than one-third of a length of the gate. The Patent Office cites Momose for this teaching. It is noted however that Momose teaches silcon dioxide (a single insulating film) may have a total thickness less than one-third of a length of a transistor gate, not a multi-layer insulating film. Regarding the rejection of claim 15, among other elements, claim 15 defines a semiconductor substrate having a transistor device formed thereon and having a gate dielectric disposed between a surface of a substrate and a gate electrode. The gate dielectric includes a first dielectric material and a second dielectric material that are scalable for feature sizes in the range of 25-20 nanometers and each having a material thickness determined by the relationship of equation (4) noted above. As noted above with respect to claim 8, the cited references fail to teach these limitations or provide any motivation for these limitations Claim 15 is not obvious over the cited references.

Claims 16-17 and 20-21 depend from claim 15 and therefore contain all the limitations of that claim. For at least the reasons stated with respect to claim 15, claims 16-17 and 20-21 are not obvious over the cited references. Applicant also notes the teachings of claim 17 relating dielectric thickness to gate length. As noted above with respect claim 10, the references fail to teach or provide any motivation for this teaching.

Applicant respectfully requests that the Patent Office withdraw the rejection to claims 8-10, 13-17 and 20-21 under 35 U.S.C. §103(a).

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Patent Office believes that a telephone conference would be useful in moving the application forward to allowance, the Patent Office is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: 11/2/05

By: William T Babbitt
William Thomas Babbitt; Reg. No. 39,591

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CERTIFICATE OF MAILING

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Nedy Calderon 11/2/05
Nedy Calderon Date

VII. CLAIMS APPENDIX

The claims involved in this Appeal are as follows:

1-7. (Canceled)

8. (Previously Presented) A transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate, the gate dielectric comprising:

a first dielectric material selected from the group consisting of HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2 and having a first dielectric constant; and

a second dielectric material having a second dielectric constant different from the first dielectric constant,

the first and second dielectric materials being scalable for a set of feature size technologies, the set of feature size technologies defined by a gate length in the range of 25-70 nm,

wherein the first material thickness and the second material thickness are determined by the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$$

wherein t_1 is the first material thickness,

t_2 is the second material thickness,

t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length,

k_1 is the dielectric constant for the first dielectric material,

k_2 is the dielectric constant for the second dielectric material, and

k_{ox} is the dielectric constant of silicon dioxide, and

wherein the transistor device is isolated from other devices by shallow trench structures.

9. (Original) The transistor of claim 8, wherein the second dielectric of the gate dielectric has a dielectric constant greater than the first dielectric constant.

10. (Original) The transistor of claim 8, wherein the first material of the gate dielectric has a first thickness and the second material of the gate dielectric has a second thickness, the combination of the first thickness and the second thickness defining a total thickness less than one-third of a length of the transistor gate.

11-12. (Canceled)

13. (Original) The gate dielectric of claim 8, wherein the second dielectric material is selected from one of BST and PZT.

14. (Original) The gate dielectric of claim 8, further comprising a third dielectric material having a third dielectric constant.

15. (Previously Presented) An apparatus comprising:

a semiconductor substrate having a transistor device formed thereon, the transistor device isolated from other devices by shallow trench structures and having a gate dielectric disposed directly between a surface of the substrate and a gate electrode comprising:

a first dielectric material selected from the group consisting of HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2 and having a first dielectric constant; and

a second dielectric material having a second dielectric constant different from the first dielectric constant,

the first and second dielectric materials being scalable for each of a plurality of feature size technologies, having a gate length in the range of 25-70 nm, and

wherein the first material thickness and the second material thickness are determined by the relationship

$$t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$$

wherein t_1 is the first material thickness,

t_2 is the second material thickness,

t_{ox} is the minimum thickness for a gate dielectric of silicon dioxide for a chosen gate length,

k_1 is the dielectric constant for the first dielectric material,

k_2 is the dielectric constant for the second dielectric material, and

k_{ox} is the dielectric constant of silicon dioxide.

16. (Previously Presented) The apparatus of claim 15, wherein the second dielectric constant is greater than the first dielectric constant.

17. (Previously Presented) The apparatus of claim 15, wherein the first material has a first thickness and the second material has a second thickness, the combination of the first thickness and the second thickness defining a total thickness less than one-third of the length of a transistor gate adapted to overly the gate dielectric.

18-19. (Canceled)

20. (Previously Presented) The apparatus of claim 15, wherein the second dielectric material is selected from one of BST and PZT.

21. (Previously Presented) The apparatus of claim 15, further comprising a third dielectric material having a third dielectric constant.

X. EVIDENCE APPENDIX

No evidence is submitted with this appeal.

XI. RELATED PROCEEDINGS APPENDIX

No related proceedings exist.